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(AY: 2024-25) May 2025 (ENDSEM) EXAM

TY (SEMESTER - II)

COURSE NAME: CMOS IC Design Branch: E&TC COURSE CODE: ETUA32204B

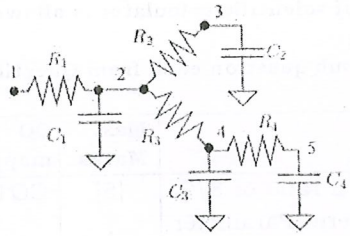
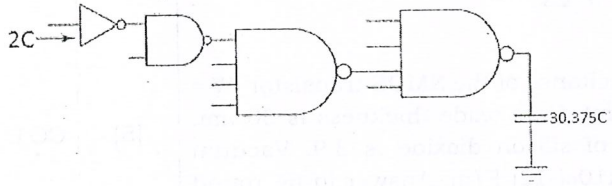
(PATTERN 2020R1)

Time: [1Hr 30 Min] **[Max. Marks: 40]**

(*) Instructions to candidates:

1) **Figures to the right indicate full marks. Use of scientific calculator is allowed**
2) **Use suitable data wherever required**
3) **All questions are compulsory. Solve any two-sub question each from Questions 1, 2 ,3 and 4**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	**a)** Consider an NMOS transistor with W/L ratio of 8/2. Calculate drain current ID in microampere. Parameter values are as follows. $\mu_n C_{ox} = 80\mu A/V^2$ $V_{Tn} = 0.5V, V_{GS} = 2V, V_{DS} = 1V$ Assume $V_{SB} = 0V$	[5]	CO1	Understand
	b) Estimate gate capacitance of the NMOS transistor (W = 1 um and L = 180 nm). Gate oxide thickness is 30 nm. Relative permittivity of silicon dioxide is 3.9. Vacuum permittivity is 8.854x10e(-12) F/m. Answer in fF, round off to 2 decimal places.	[5]	CO1	Understand
	c) Explain Body effect and channel length modulation in MOSFET with the help of neat diagram.	[5]	CO1	Understand
Q.2	**a)** Design a CMOS circuit for computing $Y = \overline{(A.B + C).D}$ Considering reference inverter has PMOS to NMOS width ratio of 2 to 1, Estimate and show the width of each transistor in the circuit. Draw the stick diagram of the circuit (Use color pens to draw the stick diagram).	[5]	CO2	Design
	b) Implement 4:1 Multiplexer using transmission gates. List the advantages and disadvantages of transmission gate over static CMOS circuits.	[5]	CO2	Design
	c) For the combinational logic circuit, CL = 100 fF, VDD = 2 V, and fclk = 2 GHz (i) Calculate switching power dissipation (ii) Calculate switching power dissipation if			

	VDD is changed to 1.5 V. Comment on the effect of supply voltage variation on switching power dissipation.	[5]	CO2	Understand
Q.3	**a)** Sketch the CMOS circuit for the function $Y = \overline{(A+B+C)\cdot D}$ and calculate the logical effort for each input. Assume (W_P/W_N) of the reference inverter is (2/1).	[5]	CO3	Apply
	b) For the RC tree structure shown below, find the propagation delay (in ps) from node 1 to node 3 using Elmore delay method. All resistances are 10 kohm and all capacitors are 1 fF. 	[5]	CO3	Apply
	c) Calculate the minimum path delay of the circuit shown below. The input inverter presents a capacitance of 2C and the output capacitance is 30.375C. 	[5]	CO3	Apply
Q.4	**a)** Draw the block diagram of 4-bit ripple carry adder. What is the propagation delay of 128-bit ripple carry adder, given the delay of carry and sum are 2 ps and 3 ps respectively?	[5]	CO4	Understand
	b) Draw the block diagram of 4-bit carry-skip adder. A 512-bit carry-skip adder is implemented using blocks of (i) 4-bits (ii) 8-bits (iii) 16-bits. Calculate the critical path delay in each case. What is the optimal number of blocks to achieve least critical path delay? Assume tGP = 3ps, tbypass = 3ps, tcarry = 3ps, and tsum = 5ps.	[5]	CO4	Understand
	c) Draw the block diagram of 3 X 3 array multiplier. Calculate the critical path delay of 8 X 8 array multiplier. Assume tAND = 2ps, tcarry = 3ps, and tsum = 5ps.	[5]	CO4	Understand